



# High Speed Digital Applications

## The Importance of Test Contactors for High-Speed Digital Device Testing

High-speed digital interfaces for the computer, consumer and communications markets have moved forward dramatically. These rapid improvements in speed and performance have created significant test challenges, requiring major changes in test methodologies and in many cases true cross-domain test approaches.

Ethernet is approaching 10Gbps on its way to 40Gbps and 100Gbps. Peripheral Component Interface (PCI express) is moving from 2.5Gbps to 5Gbps with a short-term roadmap of 8Gbps and 10Gbps.

Serial Advanced Technology Attachment (SATA) is moving from 1.5Gbps to 3Gbps with a roadmap to 6Gbps. Other network interfaces such as XAUI are already at 10Gbps and moving to 12.5Gbps, with 25Gbps on the horizon.

HDMI multimedia interface is moving from its current multi-channel 1.65Gbps to 3.3Gbps. And USB3 is headed towards 4.9 Gigabit/second speeds.

Memory interfaces are also increasing; Double Data Rate (DDR) architectures are currently running at 800Mbps and quickly moving to 1.6Gbps and 2.4Gbps and then on to 3.2Gbps, 6.4Gbps and further out 8Gbps and 16Gbps

## What Makes High-Sped Digital a Challenge?

To guarantee measurement quality of a Device Under Test's (DUT) transmit and receive signals, the interface and test instrumentation should have a bandwidth equivalent to the third harmonic of the highest frequency of interest, and in some instances the fifth harmonic.

For a 10Gbps digital signal the highest code frequency is a mark space clock type pattern, which at 10Gbps represents a 5GHz cycle/period; however, a digital signal is comprised of many frequency components (Figure 1), where the true level of speed is governed by the edge rise and fall time equivalent frequency. Therefore, the maximum bandwidth required is determined by these rise and fall times and not the base period frequency.

At 10Gbps the rise and fall times can be as low as 20ps. A bandwidth calculation from rise time is exemplified using the calculation of rise time of a step response for simple systems. To convert this rise and fall time into its -3dB equivalent bandwidth use the well known formula  $BW = 0.34 / \text{rise time}$ .

At 20ps this would indicate a fundamental -3dB frequency of 17.5GHz and a third harmonic bandwidth of 52.5GHz; not the 15GHz associated with a 5GHz sine wave, or the 5GHz pulse period. For differential signals a bandwidth equal to 1.8 times the rise time frequency is in most cases acceptable.

In this case a differential signal bandwidth of less than the 31.5GHz will tend to filter and roll off the device's signal edges. This would result in a reduced rate of change of the rising and falling edge slope; a condition that converts more of the devices random noise into jitter at the transition points, and effectively closes down the signal eyes waveform tolerance (Figures 2 & 3). As a result, good devices could potentially fail, reducing yield, revenue and profit.

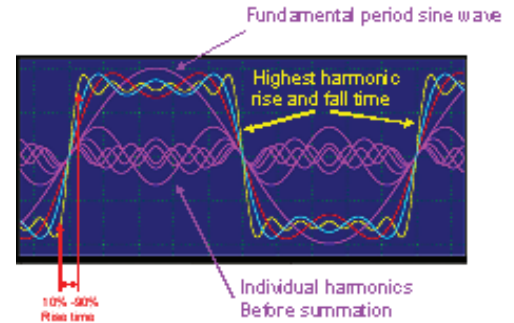


Figure 1: Multiple sine wave frequencies sum to make up a digital waveform

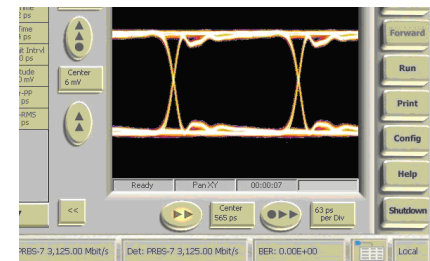


Figure 2: High Bandwidth Channel

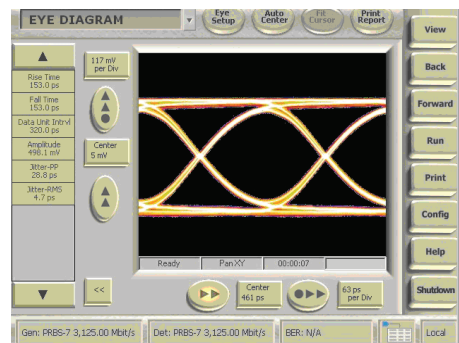


Figure 3: Restricted Bandwidth Channel

## Contactors Performance

A critical bandwidth enabler for high-speed digital signals is the test contactor; the interface between the device being tested and the loadboard. The contactor has to deal with the electrical characteristics of all the different interface connections required, and with the mechanical abuse of thousands of device packages being inserted and removed by an automated handling system.

## Electrical Challenges

The test contactor has to consider many different electrical requirements, both DC and high frequencies. These parameters include overall electrical length, contact resistance, inductance and capacitance, all of which effect operating bandwidth. For high frequency applications the contactor becomes part of an overall transmission line and therefore 'S' parameters for insertion loss, return loss and crosstalk have to be considered.

## Mechanical Challenges

A contactor also has to consider all the mechanical issues associated with device presentation and alignment. There are a number of semiconductor interconnect pitch and profile dimension tolerances, package tolerances and handling systems alignment and presentation tolerances. All these tolerances must be considered and accounted for in the overall contactor design.

To overcome these obstacles, a contactor has to provide consistent and repeatable electrical performance over a large number of device insertions, and accommodate the multiple mechanical variances. A penetration and self-cleaning mechanical action is also essential to minimize the effects of device interconnect surface oxides, test contactor contact oxide built-up and amalgamation between the contactor and the device ball material.

## Contactors Value

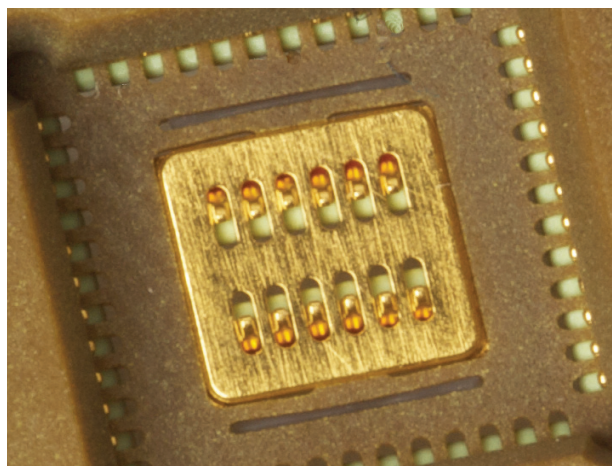
Any contactor solution must provide the necessary electrical performance required to sustain the value economics in a production environment. Value in this case is improving test throughput and cost efficiency for high performance lead-free devices, which are dependent on three major factors, test cell availability, test throughput and first pass yield quality.

Johnstech International builds products that provide superior electrical characteristics and production level mechanical performance in a lead-free environment. The result is a high performance, high reliable and low cost-of-test solution that provides a high level of customer value for high-speed digital interface semiconductor applications.

## Production Test

Johnstech Contactors provide the mechanical reliability and repeatability for production testing of IC devices necessary for maintaining higher First Pass Yields (FPY), higher overall equipment efficiency (OEE), longer mean time between assists (MTBA), and higher device throughput.

- When using multi-site handlers, Johnstech provides excellent site-site Contactor repeatability, which further enhances OEE and minimizes downtime compared to competing test socket technologies.
- Overall test performance is enhanced with repeatable Contactor performance and with an optimized handler-to-Contactor interface.
- Johnstech's worldwide support and services are available to help you achieve optimum production test performance results.



Johnstech's grounding for a Pad ROL™ 100A Series Contactor.

## Thermal and High Current

- Johnstech contacting technology utilizes solid metal contacts. The current carrying capability (CCC) is superior to non-solid contacting technologies such as spring pins. For example, even at 100% duty cycle, the ROL™ 200 contacts can handle over 4A continuous for a temperature rise of 20° C.
- Device ICs often need to dissipate several Watts of power. It is important that Contactors provide adequate thermal grounding solutions. Johnstech provides grounding solutions that include contacts-in-housing (STH, RTH), solid metal ground inserts (CI, EI), and metal inserts (SCI, RCI) with contacts installed.

## Johnstech Services

Johnstech offers a full line of technical services to assist you in achieving the highest level of performance. One of the services that is particularly powerful and effective for High Speed Digital device testing is Johnstech's use of HFSS and ADS software to model the electrical performance of the Contactor and the interface to the device and load board pads. This provides direction to select the best Contactor ground configuration for the application and to design the optimal load board trace layout, which are both vital to optimizing the overall system electrical performance. Johnstech's test floor services will help you enhance your yields, increase your performance and maintain an efficient test floor.

## Contact Johnstech

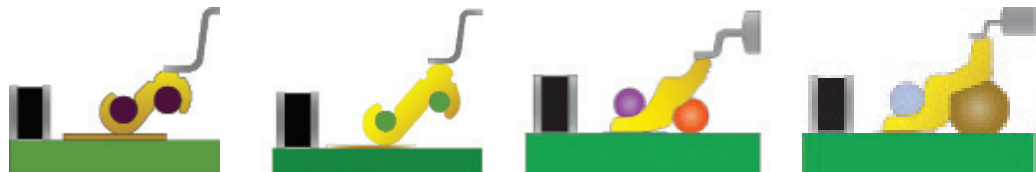
To learn more about Johnstech's patented solutions and services that maximize your High Speed Digital device testing performance, reduce your engineering risk, and provide repeatable production test results, contact your local Johnstech Sales Representative. Also learn about Johnstech parts and services at [www.johnstech.com](http://www.johnstech.com).

### Johnstech Contactors for QFN/DFN Packages



		2mm	ROL™ 200	ROL™ 100A
Inductance	Self:	0.50 nH	0.42 nH	0.23 nH
	Mutual:	0.07 nH	0.24 nH	0.14 nH
Capacitance:	Ground:	0.50 pF	0.22 pF	0.16 pF
	Mutual:	0.031 pF	0.13 pF	0.05 pF
S21 Insertion Loss		-1dB @ 11 GHz	-1dB @ 24 GHz	-1dB @ 40+ GHz
S11 Return Loss		-20dB @ 9 GHz	-20dB @ 5 GHz	-20dB @ 14.5 GHz
S41 Crosstalk		-20dB @ 14 GHz	-20dB @ 22 GHz	-20dB @ 32 GHz
Current Carrying Capability:		5.20 A	4.15 A	3 A
Contact Compliance:		0.20 mm	0.20 mm	0.175 – 0.20 mm
Testing Scenario:		Engr/LVM	Engr/HVM	Engr/HVM
Device Platings		SnPb/Mtin	SnPb/Mtin/NiPdAu	SnPb/Mtin/NiPdAu
Grounding Types		STH, SCI, EI, CI	RTH, RCI, CI, EI	RTH, RCI, CI

### Johnstech Contactors for SOIC/QFP Packages



		2mm	4mm	ROL™ 200	ROL™ 400
Inductance	Self:	0.47 nH	0.61 nH	0.42 nH	0.75 nH
	Mutual:	0.20 nH	0.27 nH	0.16 nH	0.33 nH
Capacitance:	Ground:	0.34 pF	0.92 pF	0.23 pF	0.83 pF
	Mutual:	0.15 pF	0.36 pF	0.14 pF	0.30 pF
S21 Insertion Loss		-1dB @ 15.3 GHz	-1dB @ 4.6 GHz	-1dB @ 20.7 GHz	-1dB @ 5.6 GHz
S11 Return Loss		-20dB @ 5.4 GHz	-20dB @ 1.1 GHz	-20dB @ 4.4 GHz	-20dB @ 1.6 GHz
S41 Crosstalk		-20dB @ 33.9 GHz	-20dB @ 3.0 GHz	-20dB @ 16.7 GHz	-20dB @ 4 GHz
Current Carrying Capability:		6.50 A	5.70 A	6.70 A	5.70 A
Contact Compliance:		0.20 mm	0.23 mm	0.20 mm	0.23 mm
Testing Scenario:		Engr/LVM	Engr/LVM	Engr/HVM	Engr/HVM
Device Platings		SnPb/Mtin	SnPb/Mtin	SnPb/Mtin/NiPdAu	SnPb/Mtin/NiPdAu
Grounding Types		STH, SCI, CI	STH	RTH, RCI, CI	RTH

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