Choosing Pulse Parameters for High Current Testing

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Abstract:
The stepped-up application of high-power semiconductor chips to the automotive market is a driving factor in contactor design and device test. Increasing power density and the achieving of higher energy efficiencies, coupled with smaller chip packages, are extremely challenging issues. Additionally, pulse thermal analysis and testing is becoming more complex as higher current, higher power chips come on the market. The only way to analyze these devices is to look carefully at their duty cycle, start with the maximum safe operating temperature of the die and work downward to the ambient environment.

Johnstech's contacts are solid metal, hence they can handle reasonably high current densities. This is defined as the current-carrying capacity (CCC) which is base-lined at a 100% duty cycle (continuous current flow). Duty cycle is the ratio of the time the current is ON to its combined ON + OFF time. If the current through the contacts is pulsed (duty cycle <100%). then there will be a heat-cool cycle for the contacts. Under these conditions, they can carry higher current levels when compared to their steady-state CCC. It stands to reason that a short-term (<100 micro-seconds) current pulse will have a higher CCC than a long-term (>100 microseconds) pulse. Likewise, a duty cycle <50% can handle significantly more current than one >50%.

What pulse parameters do we investigate for high current testing? They can be enumerated as follows.

- Length of the pulse (ON time)
- Peak power of the applied pulse(s)
- Duty cycle (ON time divided by ON+OFF time)
- Repetition rate of the duty cycle.
- Whether a single pulse is applied or multiple pulses (pulse train) is applied
- Operating ambient temperature

The other important factor to consider, and this is the task of the thermal analyst, is the plating material of the device pads or leads. If the current level, pulsed or continuous, is high, the interface between the device under test and the contacts must be investigated to determine if arcing or material softening will occur. In this respect, there are several techniques the thermal analyst can apply to determine the maximum safe operating level of the device under pulsed current conditions. In those cases where the maximum safe operating level of the die in the device is exceeded, the time constant of the set-up must be considered to see if shortening the pulse application time will alleviate heat build-up. Otherwise, auxiliary cooling must be applied.

Introduction:
Pulsed thermal analysis is becoming very complex as more high current, high power chips come on the market. The only way to analyze these devices is to look carefully at their duty cycle and start with the maximum safe operating temperature of the die and work downward to the ambient environment. One must consider the ON time of the device, its thermal use and how long the device needs to cool down in its OFF cycle. Let's propose a sequence of steps to be used for a typical pulse thermal analysis and include some sample calculations.

Die-to-Case:

1. Determine the maximum safe operating temperature of the die junction. Usually it is +150°C.
2. Examine the duty cycle of the device. Duty cycle is defined as…

$$\delta = t_p / T$$

   where:

   t_p is the ON time, and
   T is the length of one cycle, $T = t_p + (T - t_p) = t_{ON} + t_{OFF}$

3. Note the thermal resistance, junction-to-case, $\theta_{j\text{-}c}$ (°C/W), of the device.

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4. Will the DUT be tested with an applied single-shot pulse or will it be with a train of pulses?
5. Determine the peak power of the DUT and its length of time.
6. Consult the graph, Fig. 1, and follow the method of analysis on pages 5-7 to 5-9 of the referenced Philips document. The goal is to arrive at the junction temperature of the die, either peak or average degrees Celsius.
7. Subtract T_{j-c} from $T_{j,max}$. This is the temperature difference.

Applied Power Pulse Train Analysis:

Example:
Consider a high power, 34QFN half-bridge, buck converter packaged device with internal MOSFETs. What is the final die temperature under test characterization and production test conditions? Pertinent device parameters are:

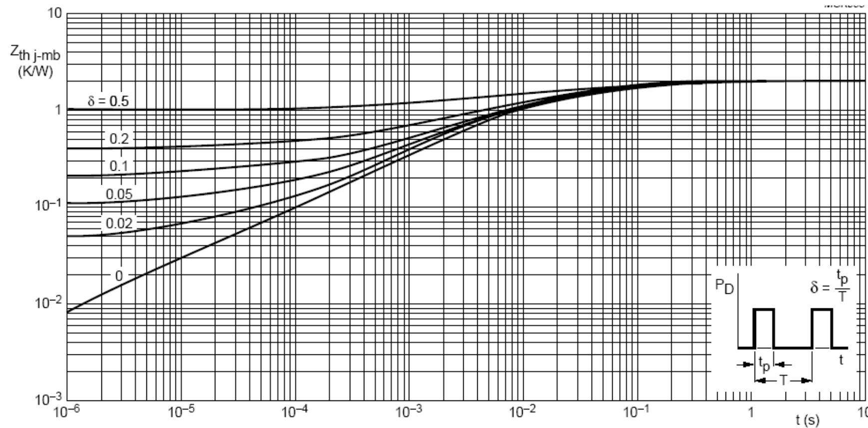
Power in = 480 Watts
Power out = 442 Watts
Power dissipated (heat) = 38 Watts
Duty cycle = 0.42 = 42%

Calculation of the die junction-case temperature (Ref. Fig. 1)
The maximum power to be dissipated (42% duty cycle, δ) is 38 Watts. Under these circumstances, 38W will be dissipated every 1.7 microseconds for a period of 4 microseconds. Refer to the chart in Fig. 1 for the following calculations. The object is to determine the thermal rise of the die junction within the mounting case. Consider the case for the die junction temperature, T_J, based on an average of the applied power:

$$P_{AVG} = P * \delta = 38 * 0.42 = 16 \text{ Watts} \quad \text{(Eq. 1)}$$
$$\Delta T_{J\text{-}MB(AVG)} = P_{AVG} * Z_{THJ\text{-}MB(\delta=1)} = 16 * 2 = 32°C \quad \text{(Eq. 2)}$$

The temperature of the die junction is;

$$T_{J\,(AVG)} = T_{MB} + \Delta T_{J\text{-}MB(AVG)} = (T_{MB} + 32)°C \quad \text{(Eq. 3)}$$



Ref: Philips Semiconductor, *Thermal Considerations*, Chpt. 5, p5-5, May 1999
Fig. 1. Graph of thermal impedance vs. pulse time/duty factor

Case-to-Loadboard:

8. If the ambient temperature is +25°C, then the difference between this value and (+150°C – T_{j-c}) is the allowed thermal rise across the test socket and the loadboard.
9. At this point, it might be worthwhile to determine the thermal impedance, R_θ, of the loadboard by using the equation,

$$R_\theta = 80 * A^{-0.7} * P_{DISS}^{-0.15} \text{ °C/Watt} \quad \text{(Eq. 4)}$$

where:

A = combined area of both sides of the loadboard

P_{DISS} = heat load (Q) to be dissipated

10. Multiply R_θ by P_{DISS} to get the temperature rise in °C across the loadboard. Subtract this value from T_{j-c} to realize the temperature rise allowed for the test socket.
    Note: There is a thermal resistance from the loadboard to $T_{Ambient}$. An average value to use for this would be 10°C/W. Add this number to R_θ and multiply by P_{DISS}. This number must be subtracted from T_{j-c} (summed with $T_{Ambient}$) to get the maximum allowed thermal rise across the test socket.
11. When the physical geometry of the test socket is decided upon, it will be possible to commence thermal synthesis in this area. The thermal and electrical resistance of the selected pin must be determined. Once the numbers are calculated, then the total thermal resistance of the test socket is determined by using this equation:

$$R\theta_{Cu\ Blk} = [(N_{pins}/\theta_{pin})^{-1} + (\theta_{CU\ BLK})^{-1}]^{-1}\ °C/W \qquad \text{(Eq. 5)}$$

$$R\theta_T = [(\theta_{Torlon})^{-1} + (N_{pins}/\theta_{pin})^{-1} + (\theta_{CU\ BLK})^{-1}]^{-1}\ °C/W \qquad \text{(Eq. 6)}$$

    Multiply $R\theta_T$ by P_{DISS} to get the temperature rise across the test socket.
12. Refer to Appendix A of this document for numerical values for the parameters shown above.

The Steady-State Case (100% Duty Cycle):

While the embodiment of this document is focused on pulse thermal analysis, it is worthwhile, as a matter of comparison, to consider the case where the DUT is being tested at a 100% duty cycle ($\delta = 1$). In this situation one would sum all the thermal impedances together as follows,

$$R\theta_T = R\theta_{j-c} + R\theta_{TS} + R\theta_{LB} + R\theta_{LB-Air} \qquad \text{(Eq. 7)}$$

and at ambient temperature (T_{AMB}):

$$T_j = T_{AMB} + (R\theta_T * P_{DISS})\ °C \qquad \text{(Eq. 8)}$$

If the value of T_j exceeds +150°C, then one must calculate the value of ΔT_{SS} and consider the problem from the standpoint of the time constant of the circuit.

Thermal Time Constant:

Let's discuss thermal time constants. For all practical purposed, there are several time constants involved. The first one to consider is the time constant, τ, of the device itself. This τ will be short and fast because the distance from a pad or lead of the case to the die is short. Any heat generated by the die will almost instantaneously reach the pad. The diffusivity will promptly transport the heat away, but it will "stack up" at the pad or lead if the ensuing thermal path has a long diffusivity. However, one must bear in mind that this only applies, in general, to power devices. Small signal devices and digital units can have thermal impedance values up to 100°C/W and beyond. As an example, suppose a DUT has a duty cycle with the following parameters (Ref: Appendix A).

$T_{ON} = 0.42 * (1/2.5x10^5) = 1.68x10^{-6}$ sec

$T_{OFF} = 4x10^{-6} - 1.68x10^{-6} = 2.32x10^{-6}$ sec

$T_S = 4x10^{-6}$ sec

$D = V_{OUT}/V_{IN} = 5/12 = 0.42$

$D = T_{ON}/T_S = 1.68x10^{-6}/4x10^{-6} = 0.42$

$\Delta T = 118°C \rightarrow$ max. allowable temperature rise

Furthermore, it is placed in a test socket whose contact pins have these characteristics.

Mass of pin:	2.616 x 10^{-6} Kg
Total thermal resistance:	152.5°C/Watt
Total electrical resistance:	3.153 milliohms

Number of contacts in housing: 23

Determine the time constant, τ, with 23 contact pins in the housing of the test socket.

$R_\theta = 152.5/23 = 6.63\Omega$

$Mass = 23*2.616x10^{-6} = 6x10^{-5}$ Kg

$\tau = m*C_P*R_\theta = 6x10^{-5} * 418.7 * 6.63 = 0.167$ sec (Eq. 9)

$\Delta T = \Delta T_{SS} * (1 - \exp(-t/\tau))$ (Eq. 10)

$118 = 373.8 * (1 - \exp(-t/0.167))$

$0.315 = \exp(-t/0.167)$

$\ln 0.315 = -t/0.167$

t = 192 milliseconds

Method 1: Determine the maximum safe operating test time for the DUT.

@250KHz (Ref: Appendix A), one (1) switching cycle is 4 microseconds long, thus:

$\#cycles = 1.93x10^{-3}/4x10^{-6} = 48,250$ cycles

Method 2: Determine the maximum safe operating test time for the DUT (Ref. Fig. 2).

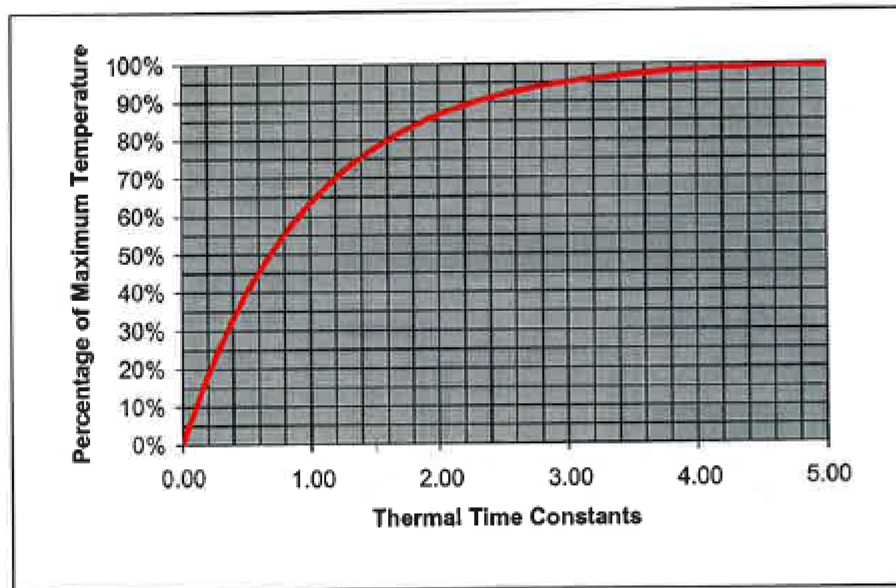


Fig. 2. Temperature Rise vs. Thermal Time Constant

Consider the thermal capacitance of the load board.

$C_{TH} = V*\rho*C_P$ J/K (Eq. 11)

where:

V = Volume, m^3

ρ = Density, Kg/m^3

C_P = Specific heat, J/kg-K

From previous analyses, the calculated time constant of the load board is 0.13 seconds.
Continuing on,

$T_{S-A(allowed)} = [150 - (32 + 25)]°C = 93°C$

$T_{S-A(max)} = 16W * 21.8°C/W = 373.8°C \rightarrow$ SS temperature rise for 100% duty cycle

Dividing the allowed $T_{S-A}$by the maximum T_{S-A} gives…

93/373.8 = 0.25 corresponds to 0.3 time constants per Fig. 2.

Consider the load board as having a time constant of 0.13 seconds, then

0.13 * 0.3 = 39 milliseconds
cycles = $39x10^{-3}/4x10^{-6}$ corresponds to 10,000 complete switching cycles

Choose this the value of safe operating time since it is the lesser of the two calculated values.

The maximum operating temperature of the die within the device is +150°C. Therefore the die temperature must not exceed +150°C, maximum. Normally, one would want a buffer zone, hence the temperature of the die should not exceed +130°C for any length of time. Another factor to consider is that the allowable safe operating limit for FR-4 material is 130°C.

Conclusions and Summary:

Pulse thermal techniques are applicable to situations where high power chips are operated in a pulsed mode with short dwell times and long cyclical periods. The cycles can either be single-shot with a low repetition rate or pulse trains. It is worth noting that if an applied pulse train is many minutes in length and the duty cycle is >25%, there is a risk that the safe die junction temperature can be exceeded. This is why a thorough thermal analysis must be conducted on the DUT, its accompanying test socket and its load board-to-ambient environment.

Details regarding pulse thermal analysis have been presented in this document. However, the reader is referred to additional work shown in Appendix A which covers essential and critical points required for analyses of this nature.

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February 14, 2011

Appendix A

Thermal Analysis For
34 QFN, Half-Bridge Buck Converter
Pad ROL™200, 138337-0001 Fine Tip
Au-Ni Plated BeCu Contacts

Abstract:
Perform thermal and high current analysis on a 34 QFN, high power, half-bridge, buck converter packaged device with internal MOSFETs. What is the final die junction temperature under test characterization and production test conditions?

Solve For:

- Heat transfer through a fine tip BeCu contact pin, Pad ROL200, plated BeCu 138337-0001
- Calculate the thermal resistance of the pad-to-contact interface
- Calculate the thermal resistance of the contact-to-LB pad interface
- Determine the total thermal resistance of the heat flow path(s)
- Determine the electrical resistance of the contact pin
- Determine the electrical resistance of the interfaces
- Determine the reliability of interfaces under high-current pulses

Given:

- A single-phase, 40 Amp buck power stage with integrated driver and fault protection.
- Input voltage is +12Volts plus ringing voltage
- Zener diodes which limit at 20 volts are built into the silicon chip to absorb surges
- Zener diodes will absorb 40 Amps of current over 10 nanoseconds per cycle
- Peak current out of the system is 40 Amps at a time duration of tens of nanoseconds per cycle
- Switching frequency is 250 KHz
- General electrical parameters:
  - Vin (max.) 12.0 V
  - Vout (min.) 0.6 V
  - Vout (max.) 5.0 V
  - Iout (max.) 40 A
  - Iout (peak) 40 A for 100×10^{-9} sec of each cycle
  - Vbias 5.0 V
  - Icc (min.) ---
  - Icc (typ.) 145 MA
  - Package type 6x6 WLCSP
  - θj-c ~3°C/W
  - θj-a ~71.4°C/W
  - t_{rr} 20.4×10^{-9}sec
  - Q_{RR} 7×10^{-9} Coulomb
  - Q_{DISS} ~38.4 Watts
  - Max. junction temp. +150°C
  - Phase pads carry 40 A
  - Efficiency (η) 0.92
  - Rds(on) lower MOSFETs 6 milliohms
  - Rds(on) upper MOSFETs 6 to 8 milliohms
- Reliability test: inductive discharges of up to 100 Amps for 1 millisecond
- Silicon die is nearly the same size as the package
- Silicon may be exposed through the top of the package. For this analysis, it is presupposed that 10% of heat goes out the top of package and 90% of heat exits through the bottom of package.

Solution and General Calculations:

Characteristics of gold-plated BeCu (138337-0001) fine tip contact pins

Material:	BeCu (C172), Au-Ni plated
	Surface roughness: $\sigma = 0.8 \times 10^{-6}$ m
	Tan $\varphi = 0.114$ at tip
	Tan $\varphi = 0.114$ at bottom
Thermal conductivity (k):	90 W/m-K
Specific heat (c_p):	418.7 J/Kg-K
Density (ρ):	8,321.4 Kg/m^3
Resistivity (σ):	7.68×10^{-8} Ohm-m
Surface area of contact pin:	1.169×10^{-6} m^2
Width of pin at tip:	$1.270 \times 10^{-4} \times 0.95 = 1.207 \times 10^{-4}$m
Width of pin at base:	$2.690 \times 10^{-4} \times 0.95 = 2.555 \times 10^{-4}$m
Cross-sectional Area of pin:	1.570×10^{-7} m^2
Volume of pin:	3.145×10^{-10} m^3
Mass of pin:	2.616×10^{-6} Kg

Force of contact against matte tin pad ~ 65 grams

Hertz stress:

- 143,322 psi for tip of pin against matte tin device pad
- 19,704 psi for base of pin against gold-plated load board pad

Thermal resistance of contact pin = 138.9°C/W

Thermal resistance of IF1 = 11.2°C/W

Thermal resistance of IF2 = 2.4°C/W

Total thermal resistance ($\theta_{IF1} + \theta_{contact\ pin} + \theta_{IF2}$) = 152.5°C/Watt

Electrical resistance of contact pin = 1.054 milliohms

Electrical resistance of IF1 = 7.567×10^{-4} ohms

Electrical resistance of IF2 = 1.342×10^{-3} ohms

Total electrical resistance ($R_{IF1} + R_{pin} + R_{IF2}$) = 3.153 milliohms

Proposed contactor pin-outs to pads of device

- Vin — 8 contacts (7-force; 1-sense)
- GND1 — 4 contacts
- GND2 — 9 contacts
- Phase 1 — 8 contacts
- Phase 2 — 0 contacts

Softening and melting voltages of matte tin and gold

- Matte Tin — Soft @ 70 mV
- Matte Tin — Melt @ 130 mV
- Gold — Soft @ 80 mV
- Gold — Melt @ 430 mV

Interface Evaluation at Vin (12V max.) @ 40 Amps

$V_{IF1} = [(40\text{ A} \times 7.567 \times 10^{-4}\text{ ohm})/(7\text{ pins})] = 4.3$ mV/pin < 70 mV required to soften tin

$V_{IF2} = [(40\text{ A} \times 1.342 \times 10^{-3}\text{ ohm})/(7\text{ pins})] = 7.7$ mV/pin < 80 mV required to soften gold

Interface Evaluation at Vout (0.6V min., 5.0V max.) @ 40 Amps

$V_{IF1} = [(40\text{ A} \times 7.567 \times 10^{-4}\text{ ohm})/(7\text{ pins})] = 4.3$ mV/pin < 70 mV required to soften tin

$V_{IF2} = [(40\text{ A} \times 1.342 \times 10^{-3}\text{ ohm})/(7\text{ pins})] = 7.7$ mV/pin < 80 mV required to soften gold

Note: If "current hogging" does not occur and the load is shared equally among the pins, then the Ifs are okay at the calculated voltages. No melting or arcing should occur.

Evaluation of the duty cycle

$T_{ON} = 0.42 * (1/2.5 \times 10^5) = 1.68 \times 10^{-6}$ sec

$T_{OFF} = 4x10^{-6} - 1.68x10^{-6} = 2.32x10^{-6}$ sec
$T_S = 4x10^{-6}$ sec
$D = V_{OUT}/V_{IN} = 5/12 = 0.42$
$D = T_{ON}/T_S = 1.68x10^{-6}/4x10^{-6} = 0.42$

Determination of heat load for MOSFETs

$I_{L,P\text{-}P} = 0.42$ Iout $= 0.42 \times 40 = 16.8$ Amps
$I_{L,P\text{-}P} = [(Vin - Vout)/(Fsw \times L)] \times (Vout/Vin)$ (Eq. A1)
$L = 1.46x10^{-6}/16.8 = 20.8x10^{-9}$ Henrys/channel

$16.8 = [(12\text{-}5)/(2.5x10^5 \times L) \times (5/12) = 0.70x10^{-6}/L$
Duty cycle = d = 5/12 = 42%
1 – Duty cycle = 1.0 – 0.42 = 0.58

Heat dissipation of 1st lower MOSFET
$P_L = Rds(on)x\ [(I_m/2)^2 \times (1\text{-}d) + (I_{L,P\text{-}P}{}^2 \times (1\text{-}d)/12)]$ (Eq. A2)
$P_L = 0.006x[(40/2)^2x(1\text{-}0.42) + (16.8^2x(1\text{-}0.42)/12)] = 1.47$ Watts

Heat dissipation of 2nd lower MOSFET
$P_D = V_{D(ON)} \times Fsw[((I_m/2) + (I_{pp}/2)) \times t_{d1} + ((I_m/2) - (I_{pp}/2)) \times t_{d2})]$ (Eq. A3)
$P_D = 0.7 \times 2.5x10^5 \times [((40/2) + (16.8/2)) \times 4.5x10^{-9} + ((40/2) - ((16.8/2)) \times 4.5x10^{-9})]$
$P_D = 0.21$ Watts

Total heat dissipation (Q) of lower MOSFETs = $P_L + P_D$ = 1.47 + 0.03 = 1.50 Watts

Heat dissipation of upper MOSFETs
$P_{UP,1} \approx Vin\ x[((I_m/2) + (I_{pp}/2))x(t_1/2)xFsw]$ (Eq. A4)
$P_{UP,1} \approx 12 \times [((40/2) + (16.8/2)) \times (16.7x10^{-9}/2)x2.5x10^5 = 0.71$ Watts

$P_{UP,2} \approx Vin\ x[((I_m/2) - (I_{pp}/2))x(t_2/2)xFsw]$ (Eq. A5)
$P_{UP,2} \approx 12 \times [((40/2) - (16.8/2)) \times (16.7x10^{-9}/2)x2.5x10^5 = 0.29$ Watts

$P_{UP,3} \approx Vin \times Qrr \times Fsw$ (Eq. A6)
$P_{UP,3} \approx 12 \times 7x10^{-9}\ x2.5x10^5 \approx 0.02$ Watts

$P_{UP,4} \approx Rds(on) \times ((I_m/2)^2xd + (I_{pp}{}^2/12))$ (Eq. A7)
$P_{UP,4} \approx 0.008 \times ((40/2)^2 \times 0.42 + (16.8^2/12)) = 1.53$ Watts

Total heat dissipation (Q) of upper MOSFETs = $P_{UP,1} + P_{UP,2} + P_{UP,3} + P_{UP,4}$
= 0.71 + 0.29 + 0.02 + 1.53
= 2.55 Watts

Consider the power requirements to the rest of the chip as 100mA x 5 V = 0.5 Watts and adding safety factor of 1.5, thus the

Total heat load = 1.5(1.50 + 2.55 + 0.5) = 6.8 Watts
In summation, to this point:

Phase 1:	8 pins will carry 40 Amps total @ 5V = 5.0 Amps/pin
Phase 2:	N/A
LH GND:	9 pins will carry 27.7 Amps total @ 0V = 3.1 Amps/pin
RH GND:	4 pins will carry 12.3 Amps total @ 0V = 3.1 Amps/pin
Control Ckts:	Negligible V and A (in comparison to the power circuitry)
+Vin:	7 pins will carry 40 Amps total @ 12V typical
Shock Test:	4 pins will carry 100 Amps total at 25 Amps/pin
	Note: 20V (limited by Zener diode) = 2KW for 30 microseconds at

several pulses per cycle.

Thermal Calculations For Die Temperature

$Q = 6.8$ Watts
$\theta_{j\text{-}c} = 3°C/W$
$\theta_{j\text{-}top} = 4.44°C/W$
$\theta_{j\text{-}bottom} = 40°C/W$
$\theta_{hs\text{-}air} = 5°C/W$ est.

If 90% the heat exits the bottom of the package through the pins and contactor, then

The thermal impedance of Torlon housing (w/23 pins) and a copper insert is:

$$\theta_T = [(\theta_{Torlon})^{-1} + (N_{pins}/\theta_{pin})^{-1} + (\theta_{CU\ BLK})^{-1}]^{-1}\ °C/W \qquad \text{(Eq. A8)}$$

$$\theta_T = [(1/121) + (23/152.5) + (1/5)\ ]^{-1} = 2.8°C/W$$

Thermal analysis of half-bridge, buck-boost circuit (Ref. Fig. 1)

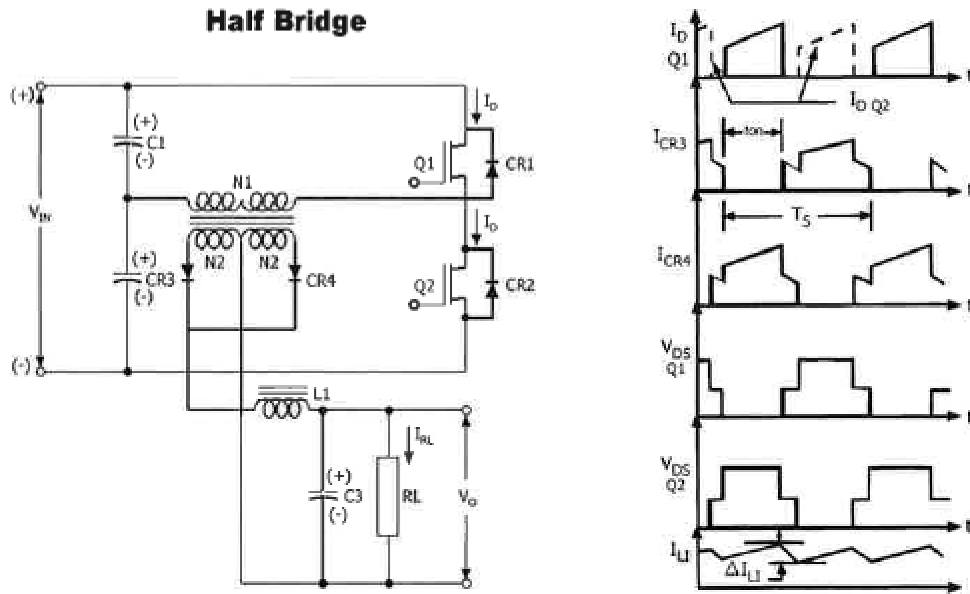


Fig. 1. Simplified schematic diagram of half-bridge, buck-boost circuit with current and voltage waveforms.
Ref. www.intersil.com/engineering tools

Given:

$P_{IN} = 480$ Watts
$P_{OUT} = 442$ Watts
$Q_{DISS} = 38$ Watts of heat
$Q_{DISS,\ MOSFETs} = 4$ Watts of heat
$Q_{DISS} - Q_{DISS,\ MOSFETs} = 34$ Watts of heat

Calculation of the die junction-case temperature (Ref. Fig. 1)

Applied Power Pulse Train Analysis:

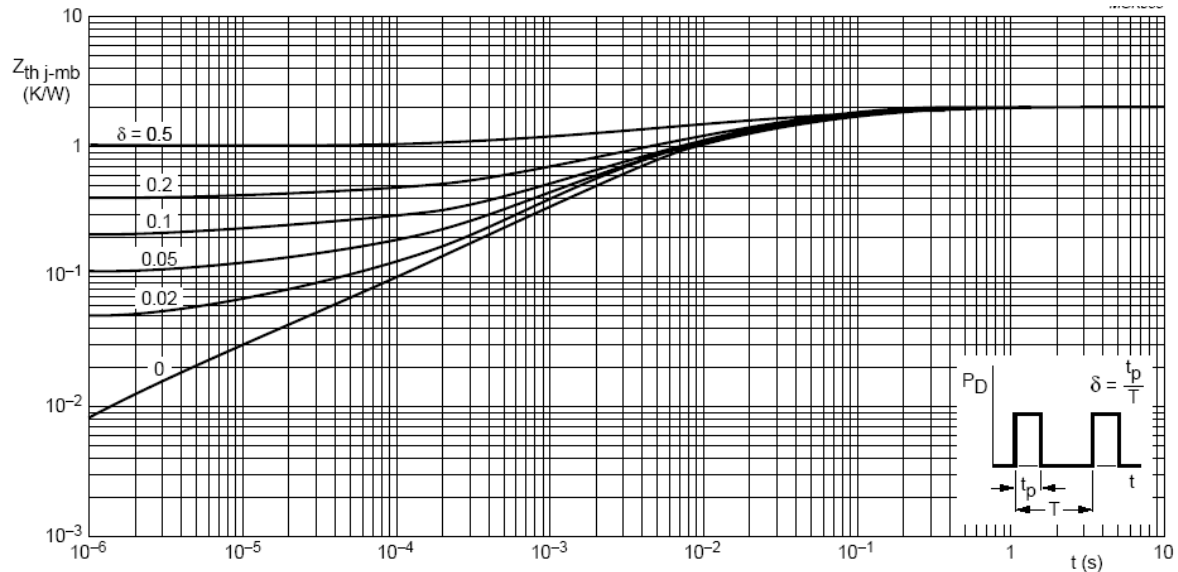
The maximum power to be dissipated (42% duty cycle) is 38 Watts. Under these circumstances, 38 Watts will be dissipated every 1.7 microseconds for a period of 4 microseconds. Refer to the chart in Fig. 2 for the following calculations. The object is to determine the thermal rise of the die junction within the mounting case. Consider the case for the die junction temperature, T_J, based on an average of the applied power:

$$P_{AVG} = P * \delta = 38 * 0.42 = 16 \text{ Watts}$$

$$\Delta T_{J\text{-}MB(AVG)} = P_{AVG} * Z_{THJ\text{-}MB(\delta=1)} = 16 * 2 = 32°C \qquad \text{(Eq. A9)}$$

The temperature of the mounting base is then,

$$T_{J\,(AVG)} = T_{MB} + \Delta T_{J\text{-}MB(AVG)} = (T_{MB} + 32)°C \qquad \text{(Eq. A10)}$$



- Ref: Philips Semiconductor, *Thermal Considerations*, Chpt. 5, p5-5, May 1999

Fig. 2. Graph of thermal impedance vs. pulse time/duty factor

Thermal Impedance of PC Board-to-ambient environment:
Given a typical size of the PCB (4.5”x4.5’x0.010”) for this test setup, it is reasonable to consider it as a flat plate, thus the thermal resistance of a flat plate to a first order approximation (±10%), is

$$R_\theta = 80*A^{-0.7}*P^{-0.15} \qquad \text{(Eq. A11)}$$

Where:

R_θ = thermal resistance in °C/W
P = power in Watts (heat load)
A = area in square inches (including both sides)

Since the printed circuit board is coated with 1 ounce copper, spreading resistance (lateral resistance to heat flow) becomes a consideration, whereby the heat flow through the copper foil decreases with distance thereby causing radiation to the air, and also the temperature, to decrease measurably with distance from the heat source. In this case, the 1 ounce copper effectively limits the heat sinking to less than a 2 inch circle.

For an effective two-sided area of the printed circuit board of 6.3 square inches, the thermal resistance is calculated to be:

$$R_\theta = 80*12.5^{-0.7}*16^{-0.15} = 9.0°C/W$$

This value of thermal resistance will become part of the overall calculations to determine die temperature later in this paper.

Refer to Fig. 3 immediately below:

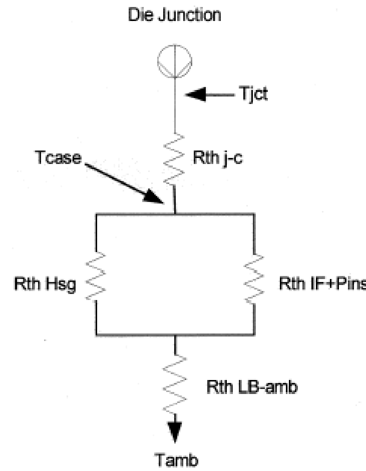


Fig. 3. Schematic diagram of DUT-to-T_{AMB} thermal resistance

Where,

- Rth,j-c = θj-c = thermal resistance, die junction to case
- Rth,if-pins = θif-pins = thermal resistance, interfaces + pins
- Rth,hsg = θhsg = thermal resistance of socket housing
- Rth,$_{LB}$-amb = θ_{LB}-amb = thermal resistance, load board to ambient air
- $\theta Total = \theta j\text{-}c + [\theta if\text{-}cp \parallel \theta_{hsg}] + \theta_{LB\text{-}Amb}$

Use the following numerical values in conjunction with Fig. 2

- P_D = 16 Watts
- $T_{J\text{-}C}$ = 32°C
- θhsg ‖ θif-pins = 2.8°C/W
- θ_{LB}-amb = 19°C
- T_{AMB} = +25°C
- T_{CASE} = 150 – 32 = 118°C

Now consider the temperature of a die within the device at ambient temperature when given the following conditions.

- Heat load (Q): = 16 Watts
- $\theta_{jc\text{-}bottom}$ = 40°C/W Estimated
- R_θ = 21.8°C/W
- Test time: ~ TBD seconds

@ T_{AMB} = +25°C: T_C = +25 + (16*21.8) = 373.8°C; which is excessive, but is the final Steady-State value.

Determine the time constant, δ, by considering 23 contact pins.

$R_\theta = 152.5/23 = 6.63\Omega$
Mass = $23*2.616\text{x}10^{-6} = 6\text{x}10^{-5}$ Kg
$\delta = m*C_P*R_\theta = 6\text{x}10^{-5} * 418.7 * 6.63 = 0.167$ sec

$$\Delta T = \Delta T_{SS} * (1 - \exp(-t/\delta)) \quad \text{(Eq. A12)}$$
$$118 = 373.8 * (1 - \exp(-t/0.167))$$
$$0.315 = \exp(-t/0.167)$$

$$\ln 0.315 = -t/0.167$$
$$t = 192 \text{ milliseconds}$$

Method 1: Determine the maximum safe operating test time for the DUT.

@250KHz, one (1) switching cycle is 4 microseconds long, thus:

$$\#cycles = 1.93x10^{-3}/4x10^{-6} = 48{,}250 \text{ cycles}$$

Method 2: Determine the maximum safe operating test time for the DUT (Ref. Fig. 4).

Consider the thermal capacitance of the load board.

$$C_{TH} = V*\rho*C_P \quad J/K \qquad \text{(Eq. A13)}$$

where:

V = Volume, m^3
ρ = Density, Kg/m^3
C_P = Specific heat, J/kg-K

From previous analyses, the calculated time constant of the load board is 0.13 seconds.

Continuing on,

$$T_{S\text{-}A(allowed)} = (150 - 32 - 25)°C = 93°C$$
$$T_{S\text{-}A(max)} = 16W * 21.8°C/W = 373.8°C$$

Dividing the allowed $T_{S\text{-}A}$ by the maximum $T_{S\text{-}A}$ gives…

93/373.8 = 0.25 corresponds to 0.3 time constants per Fig. 4.

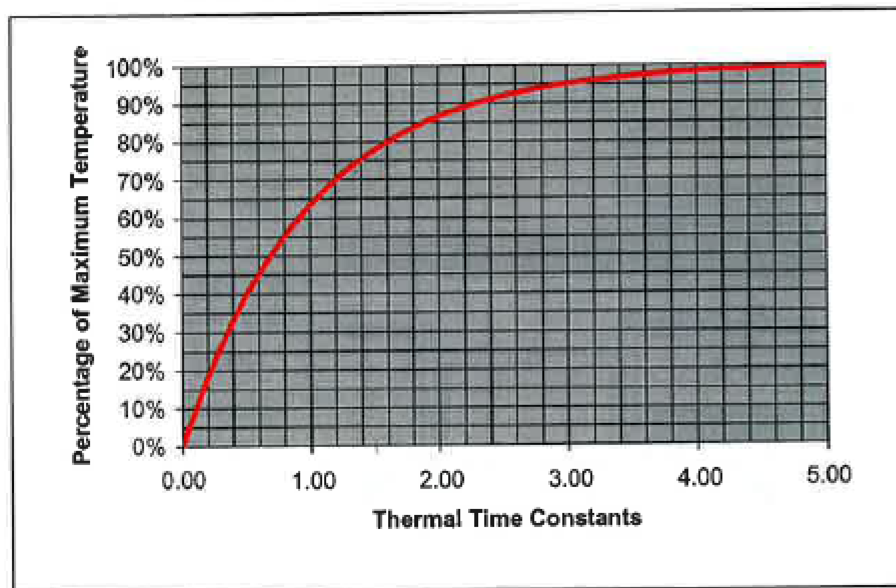


Figure 4. Temperature Rise vs. Thermal Time Constant

Consider the load board as having a time constant of 0.13 seconds, then

$$0.13 * 0.3 = 39 \text{ milliseconds}$$
$$\# cycles = 39x10^{-3}/4x10^{-6} \text{ corresponds to 10,000 complete switching cycles}$$

Choose this value of safe operating time since it is the lesser of the two calculated values.

The maximum operating temperature of the die within the device is +150°C. Therefore the die temperature must not exceed +150°C, maximum. Normally, one would want a buffer zone, hence the temperature of the die should not exceed +130°C for any length of time. Another factor to consider is that the allowable safe operating limit for FR-4 material is 130°C.

Summary and Conclusions:

The purpose of this analysis was to determine if the packaged device could safely operate at a test temperature range of +25°C while dissipating a heat load of 16 Watts. In this vein, it has been determined that the device could operate in a test socket for approximately 39 milliseconds (10,000 switching cycles) before it must be turned off and allowed to cool down. The cool-down period must be at least five (5) time constants or 650 milliseconds.

Another aspect of this analysis was to determine if the device would work in the test socket with a pulsed shock current of 100 Amps applied to the voltage input terminals for a brief period of up to 30 microseconds. This has been addressed as the above analysis shows. Some caveats apply as noted above.

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