IQtouch™ Wafer Test (Probe) Application Brief

CRITICAL TEST PARAMETERS FOR POWER MANAGEMENT (PMIC) DEVICES

A standard PMIC typically consists of several SMPS (Switch Mode Power Supply) converters with different output voltage, current and power ratings (see Figure 1). Among the key performance specifications are conversion efficiency, line and load regulation, transient response and ripple, all of which affect battery life.

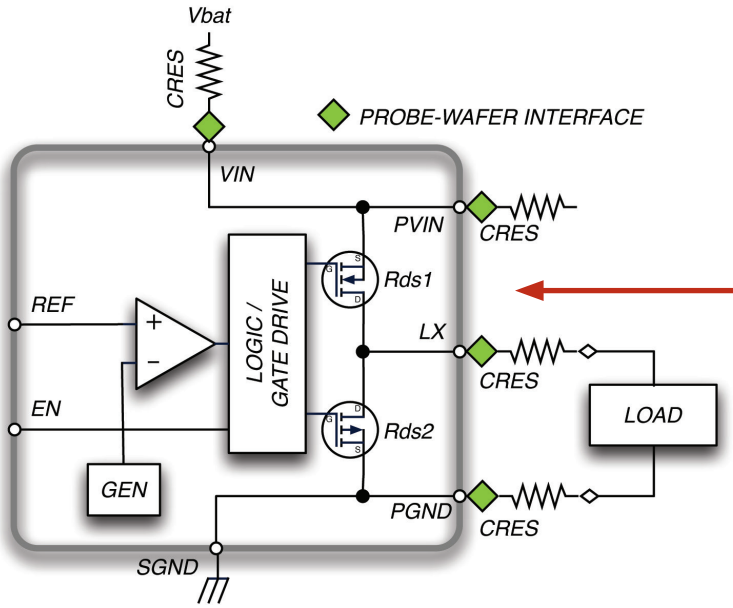


Figure 1: Typical Step-down SMPS Output Stage

Critical Test Challenges

Accurate and consistent measurement of voltage, current and time domain are necessary features for both pre-launch device validation and production test.

Consider an important component of a buck converter for efficiency and output power measurements known as high side (Rds1) conduction loss:

$P_{cond} = I^2 \times R_{dson} \times V_{out}/V_{in}$,

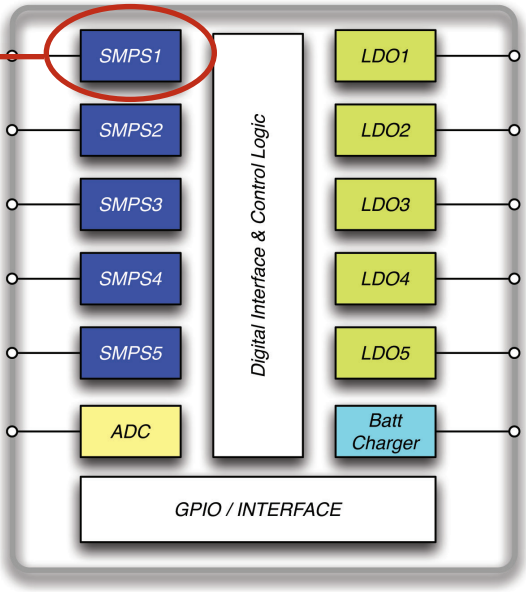
where P_{cond} = conduction loss

I = output current

R_{dson} = FET source-drain ON resistance

V_{out} = converter output voltage

V_{in} = battery supply voltage



Critical Test Parameters:

- **Conversion Efficiency**
- **Line and Load Regulation**
- **Transient Response/Ripple**

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IQtouch™ Advantage

The Johnstech IQtouch™ probe array's CRES behavior in actual production tests (green graph in Figure 3) provides consistently tight distribution compared to a typical spring pin probe solution (purple graph in Figure 3). These results demonstrate a potential IQtouch™ competitive advantage in both device validation and product test environments, and will improve test reliability, time-to-market, and production yields.

Major production impact:

- **Higher FPY (First Pass Yield) of 2% – 3%**
- **Higher Cpk allowing wider test limit margins**
- **Less Retest and False Failures**
- **Lower total cost of test**

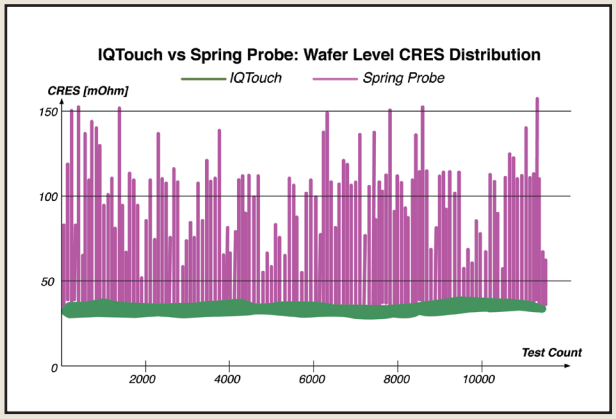

Figure 3: Actual customer WLCSP CRES distribution of IQtouch™ (green) vs Spring Probe (purple)

The conduction loss equation shows the direct relationship between conduction loss and the accurate representation of R_{dson}, V_{out}, V_{in} and I. Given the simplified ATE measurement setup (see Figure 2) that takes into account the probe contact resistance (CRES), any variation of IR voltage drop between the ATE and the DUT will negatively impact test measurement accuracy and repeatability. If CRES is taken into account for each affected parameter in the conduction loss equation, such as R_{dson} and voltage measurements, high variance CRES measurements will clearly result in inaccurate test results. This could lead to unnecessary downgrading of device specifications and loss of production yield.

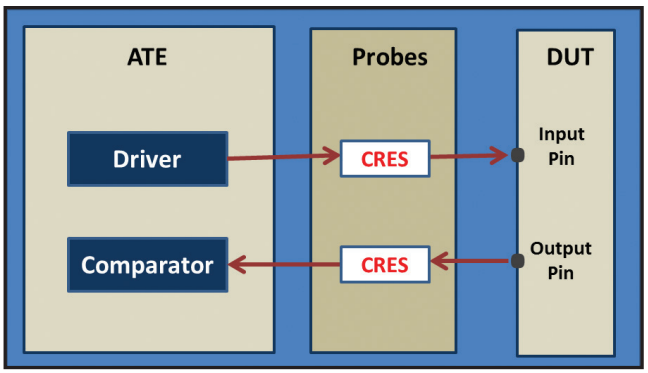

Figure 2: Simplified ATE Measurement

Johnstech Engineering Services

Test engineers rely on Johnstech to reduce risk, shorten development, and improve first pass yields. Johnstech provides test floor consultation, electrical modeling, thermal modeling and load board/probe card optimization services.

Contact Johnstech

To learn more about Johnstech's patented solutions and services that maximize your PMIC, RFIC, and SOC testing performance, reduce your engineering risk, and provide repeatable production test results, contact your local Johnstech Sales Representative or send an email to probe@johnstech.com. Learn about Johnstech Wafer Test Solutions at www.johnstech.com/IQtouch.

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