IQtouch™ Wafer Test (Probe) Application Brief

CRITICAL TEST PARAMETERS FOR RFIC DEVICES

Test hardware resources are constantly challenged by the increasing test requirement complexity of mobile RF devices, especially those designed for the mobile market. Higher levels of integration with multiple radios and RF bands, combined with more complex digital control circuitry, require a test environment that provides maximum transparency to the DUT's functional test performance. In other words, test signal integrity is absolutely critical.

Critical Test Challenges

Consider a WLAN 802.11ac RF devices with an embedded PA as shown in Figure 1 below. Accurate and repeatable measurements involving key power amplifier parameters such as output power, Power Added Efficiency (PAE), power versus time (PvT) and power on/off ramp tests require consistent and repeatable load impedance and drive parameters. As an example, consider the variables that determine PAE in the following equation:

PAE (%) = (RF Pout – RF Pin) / DC Power Supplied

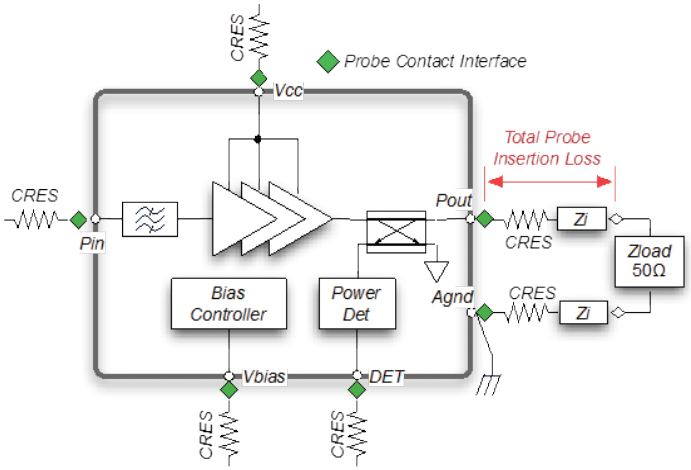

Figure 1: Typical RF SOC PA Stage Architechture. (Presented as DUT).

Critical Test Parameters:

- **Output Power**
- **Power Added Efficiency (PAE)**
- **Power vs Time (PvT)**
- **Power ON/OFF Ramps**

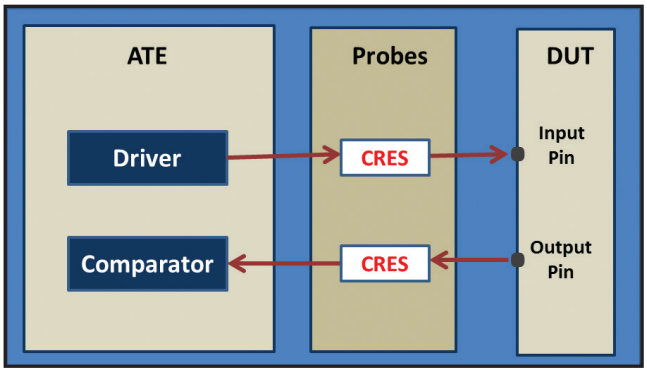

Figure 2: Simplified ATE Measurement

As implied by the simplified ATE diagram above (see Figure 2), the wafer test probes must be as transparent as possible to the test system's resources.

The RF strip lines of the DIB (Device Interface Board) are usually designed to provide a constant 50Ω impedance as seen by the DUT's RF input and output pins. Similarly, the power supply, PA bias control, and power detector pins need to have consistent impedance profiles in order to provide accurate and repeatable test results.

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IQtouch™ Advantage

The Johnstech IQtouch™ probe array's CRES behavior in actual production tests, as shown on the right (see the green graph in Figure 3), provides <50mΩ with tight distribution. Compare this to a typical spring pin probe that has >50mΩ average CRES with significant variance up to twice the average value (see the purple graph in Figure 3). Consistent and predictable CRES behavior guarantees accurate power measurements and therefore much higher FPY (First Pass Yield) with substantial reduction of retests and test escapes.

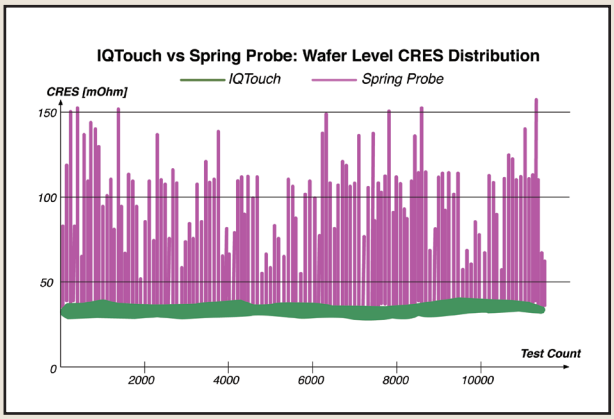

Figure 3: Actual customer WLCSP CRES distribution of IQtouch™ (green) vs Spring Probe (purple)

Key wafer probe performance specifications that provide significant impact on test accuracy and repeatability are:

1. **CRES (Contact Resistance)** — Large variances of CRES tend to generate inconsistent and often erroneous test results, affecting the RF power measurements due to impedance mismatch condition.
2. **Probe Return Loss and Insertion Loss** — Determines accuracy of input and output power measurements.
3. **Probe Jitter** — Poor and inconsistent jitter characteristics can provide erroneous PvT and power ramp measurements.

Managing Probe RF Strip Line Losses

Given the erratic behavior of spring pin probe CRES in addition to the high return loss and insertion loss characteristics, the total load impedance seen by the DUT becomes unpredictable for every probe landing, particularly at frequencies 5GHz and higher. Figures 4 and 5 show a comparison of IQtouch™ Micro vs. spring pin probe for the two most important S-parameters, insertion loss and return loss. Spring pin probes (see red line data) are a relatively longer, multi-piece technology. The higher performance of the IQtouch™ Micro (see green and blue line data) result from it being a relatively shorter, rigid probe design. The spring pin technology combination of widely varying CRES (see figure 3) and higher S-parameter losses will result in inaccurate RF power measurements, lowering first pass yield and causing higher test costs.

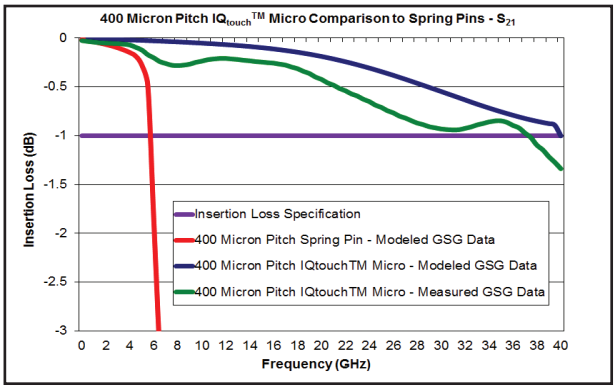

Figure 4: Insertion Loss (GSG) of IQtouch™ Micro modeled (blue) and measured (green) data vs. Spring Pins (modeled in red)

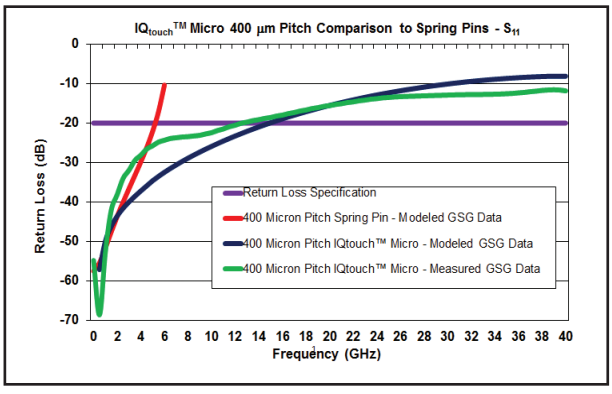

Figure 5: Return Loss of IQtouch™ Micro modeled (blue) and measured (green) data vs. Spring Pins (modeled in red).

Power and Time Measurements

Power versus Time (PvT) and power ramping test measurements are additional key parameters for 802.11ac RF devices to satisfy regulatory compliance requirements. The ramp and ON/OFF test signals are usually transmitted through the Vbias pin of the TX amplifier, and the results are measured at the Pout pin. These tests require accurate and low jitter time strobe characteristics to ensure precise time markers. For 802.11ac the power ON / OFF ramp tests have 400nsec time mask guard intervals (see Figure 6). This implies that using 1nsec least count accuracy to prevent strobe measurement errors could lead to false adjacent channel test measurements.

The Johnstech IQtouch™ Micro eye diagram (see Figure 7) exhibits the required low jitter characteristics with 10psec response resolution. Compare that to typical spring pin probe behavior (see Figure 8). Clearly, IQtouch™ provides ample accuracy margins. Time mask measurement errors may cause multiple test escapes that require further retests, with the worst case scenario being end-customer generated re-sorts.

Johnstech Engineering Services

Test engineers rely on Johnstech to reduce risk, shorten development, and improve first pass yields. Johnstech provides test floor consultation, electrical modeling, thermal modeling and load board/probe card optimization services.

Contact Johnstech

To learn more about Johnstech's patented solutions and services that maximize your PMIC, RFIC, and SOC testing performance, reduce your engineering risk, and provide repeatable production test results, contact your local Johnstech Sales Representative or send an email to probe@johnstech.com. Learn about Johnstech Wafer Test Solutions at www.johnstech.com/IQtouch.

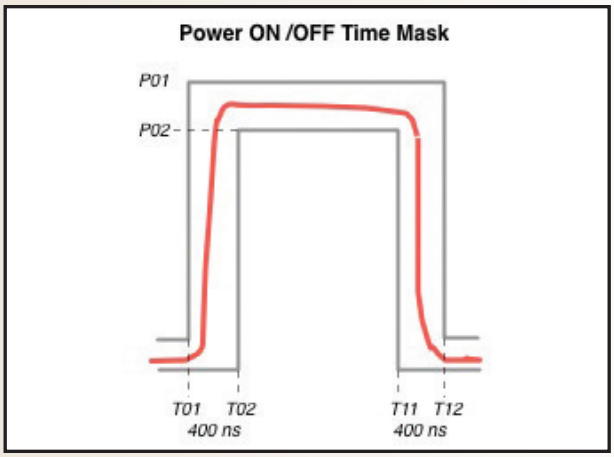

Figure 6: Power On/Off Time Mask Chart.

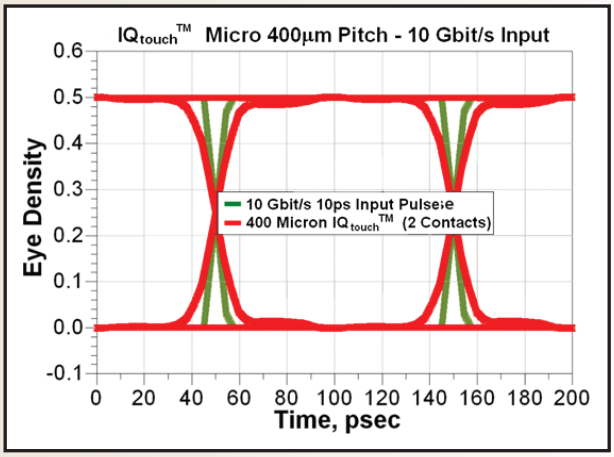

Figure 7: IQtouch™ Micro Eye Diagram.

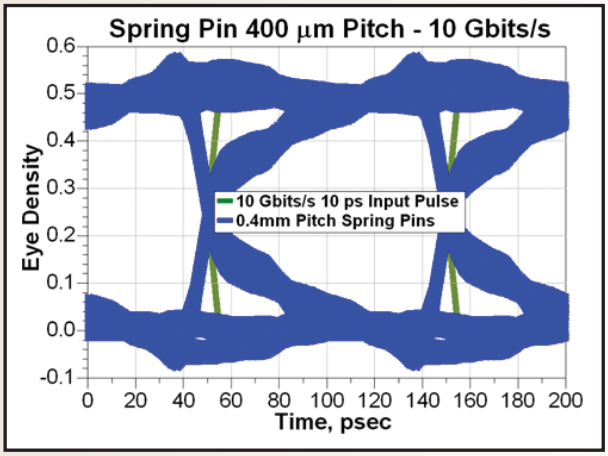

Figure 8: Spring Pin Eye Diagram.

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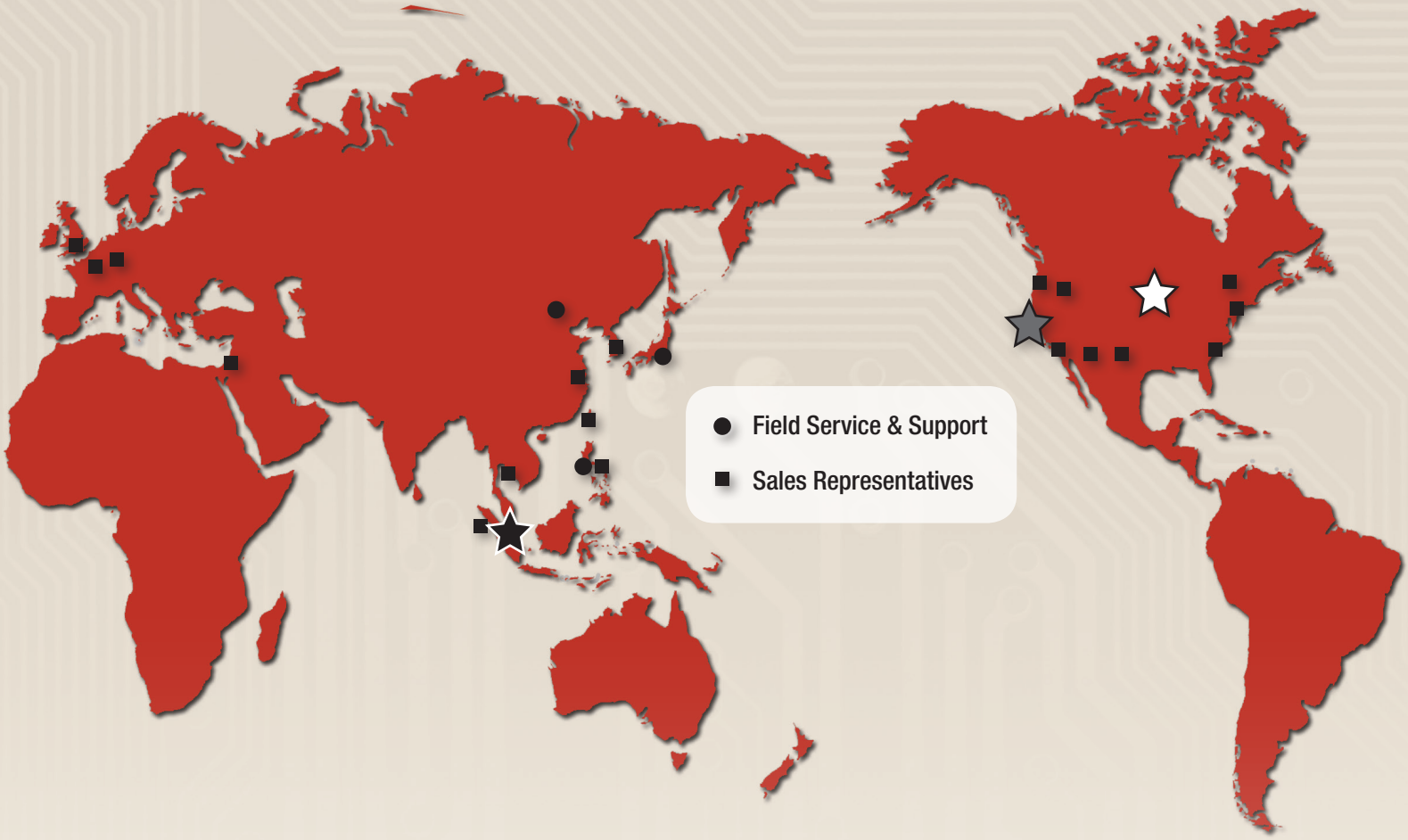

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