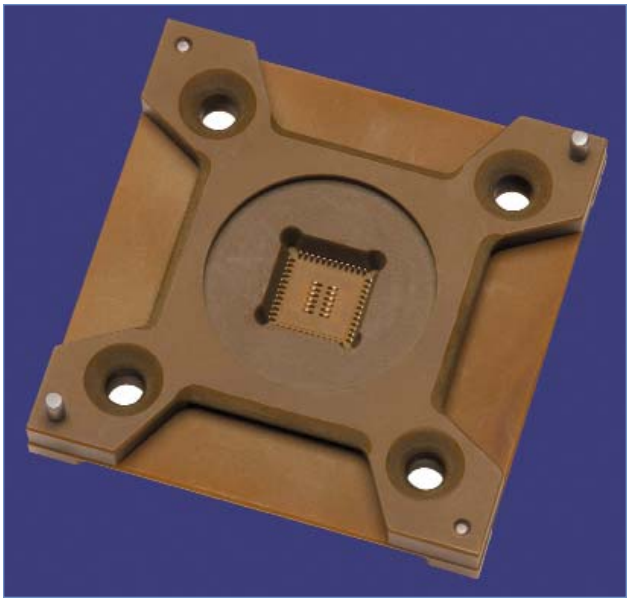
Understanding How Pb-Free Platings Affect Production-Test Cost, Throughput and Yield

Although much work has been done to create lead-free solder platings, less energy has been devoted to the final testing of these new, lead-free packaged devices. Achieving and improving on previous tin-lead throughput levels requires an understanding of lead-free plating issues, as well as a change in contactor design.

By Bert Brost and Harlan Faller, Johnstech International, Minneapolis, Minnesota, [johnstech.com]



The production of lead-free contactors requires an understanding of the many issues involved in device plating.

New, lead-free device input/output platings are reducing throughput and increasing the total cost of test in the semiconductor industry. Accordingly, it has become critical that users understand how to reduce test costs and increase test throughput and yield.

The most common Pb-free platings today are matte tin (Sn) and nickel-palladium-gold (NiPdAu). The extreme hardness of NiPdAu, can prematurely wear contact pins and transfer excessive forces to load boards, which results in time lost to maintenance and the need for load board replacement (Figure 1).

The premature wear of contact pins may also result in lower yields due to worn pins that provide poor electrical and mechanical interconnect to the device I/O.

Contact Resistance

Oxide-rich matte tin causes increased and highly variable contact resistance, resulting in lower yields.

Matte tin solder quickly builds up on the contact pins, which causes yields to fall, due to the increased variability of contact-pin resistance values. While more frequent cleaning seems to counter the oxide buildup of matte tin, the increased contactor cleaning may also result in a throughput drop.

Factors for Pb-free Performance

Before discussing solutions, one must first consider the influencing factors of Pb-free production-test contacting. The contactor features and Pb-free plating factors that contribute to the overall test performance consist of:

- Plating interactions
- True surface area
- Plating oxides
- Insertion and withdrawal forces
- Mechanical force control

Plating Interactions

One of the guidelines of interconnect plating is to avoid mixing gold with tin, because a similarity in their structures causes certain gold and tin elements to amalgamate and form an alloy.

Usually, heat (either applied or current-developed) must be present for tin-gold alloys to form. In a static situation, alloys can form over time, due to the diffusion of one material into the other.

In a dynamic condition, such as contactor pins repeatedly contacting devices in production test, the larger issue is breaking or wiping through the tin oxides to form a good, low-resistance electrical connection.

Contact pins fabricated from heavy precious metal elements or combinations of suitable elements will create a contact pin that is both highly conductive and resistant to forming a crystalline structure with tin.

If gold-plated pins are used with tin alloy solders, these pins should include a mechanism for self-cleaning. The self-cleaning function will help retard the progress of amalgamation between the gold plating and tin. Plated pins should be designed and plated to make sure the plating does not fatigue, crack or flake, exposing the contact-pin base metal.

Surface Asperities and Surface Area

The greater the conducting surface area, the lower the contact resistance. All current-carrying contact occurs at the point where a surface's asperities (irregularity peaks) touch each other (Figure 2).

Naturally, the greater the surface area and applied force, the more surface asperities touch and plasticize to form the true contact surface area.

Surface roughness, however, is somewhat of an ambivalent factor since the key issues are the forces involved as well as

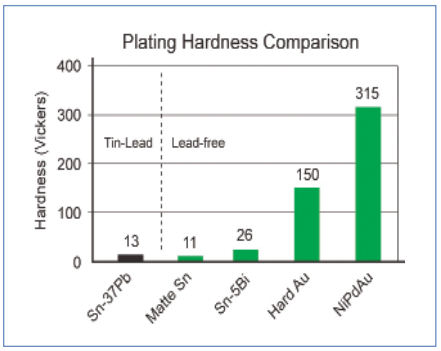


Figure 1. Hardness comparison between I/O platings

the number of asperities in contact (Figure 3).

It is important to understand that the first surface on tin-plated device pads and leads consists mostly of oxides. The contact pin must displace the oxides to create the new (almost oxide-free) true contact surface area that is required for low contact pin-to-I/O resistance.

In fact, the apparent contact area and true contact area are not the same. The true contact area is the quotient of the applied contact load divided by the hardness of the materials, with the understanding that the softer material yields, since its asperities deform and flatten under compression.

Deformation Behavior

Asperity fundamental deformation behavior (the development of the true contact area) can be modeled and analyzed to determine interaction between the contact pin surface and Pb-free device surface.

This modeling and analysis allow contact-pin tips to be optimized for both low contact resistance and low contact resistance variability. The same method can be used to model solder buildup on single (or even multiple) points of a contact pin and may be employed to project the number of devices that can be tested before cleaning is required.

Results are reported as the contact resistance average and the standard deviation of contact resistance within a sample or population of tested devices (Figure 4).

Dealing with Device-Plating Oxides

The increased oxide buildup on matte tin I/O platings makes this issue especially important for Pb-free device test.

NiPdAu generates almost no oxides, so there may only be minimal surface contamination. A concentrated pressure (force per unit area) is required to break through the oxides present on both the tip of the contact pin and the pad or lead of the device.

The pressure applied and the contact tip geometry must penetrate the oxides to form the desired amount of true contact surface area without exposing the device leadframe.

Contact pins that use a point to puncture the oxide layer are more likely to penetrate through to the leadframe, especially if forces are not tightly controlled. Contacts that wipe across the surface of the I/O will remove oxides from the I/O and contact the tip on every test.

The geometry of the wiping contact pin and the contactors' built-in motion and force controls are critical in the prevention of leadframe exposure.

Insertion and Withdrawal Forces

Contact pin insertion and withdrawal force constitutes a hysteresis curve or loop. The confined area of the loop is dependent on the characteristic of the force-biasing mechanism and the contact dynamics.

Ideally, the loop will be narrow; an area of zero is the unachievable ideal. The defining factor is the force registered at the bottom of the compliant range, with both a minimum and maximum value. The true surface area is determined by:

- The amount of applied force (how much the surface asperities plasticize and touch)
- The contact pin surface area
- The contact pin travel on the device I/O

The objective is to produce the "right" amount of force working in conjunction with the other contact pin dynamics to create the amount of true contact surface area necessary to generate repeatable, low resistance on all device I/Os and for every device tested.

The Force-Biasing Mechanism

Mechanical force control is dependent on the pin action in combination with the force-biasing mechanism. The biasing mechanism must provide adequate force to create the desired true contact surface area and to maintain low contact resistance.

The angle of the contact pin is important in helping prevent damage to the load board or device I/O. The more directly a contact-pin transfers forces to the load board or device, the more likely it is that damage will occur.

The angle of the contact pin is important in helping prevent damage to the load board or device I/O.

Improving Throughput

The topics described so far are contactor features and factors that contribute to the overall performance standards of Pb-free production test.

When preparing for or improving Pb-Free production test throughput, the practical application of these standards brings increased throughput.

The three most common productivity measures impacted by testing Pb-free

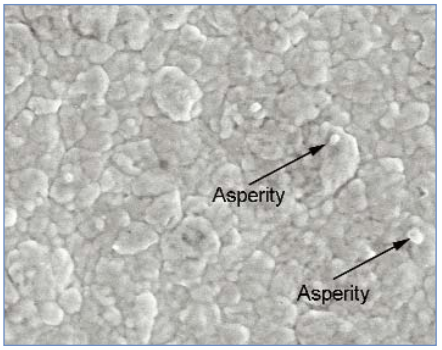


Figure 2. This 5000x SEM of tin-lead device plating reveals asperities.

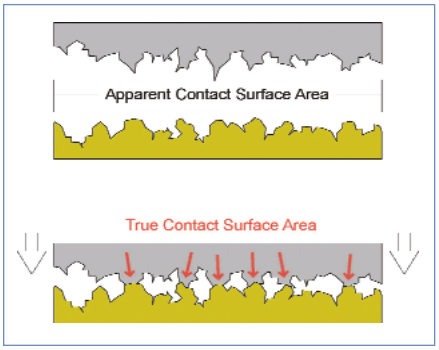


Figure 3. Illustration depicts actual vs. true contact surface area. The first surface on tin-plated device pads and leads consists mostly of oxides, which the contact pin must displace to create the new, almost oxide-free, true contact surface area needed for low contact pin-to-I/O resistance.

devices are test-cell availability rate, performance rate and quality rate.

Availability Rate

Test cell availability rate is system uptime. This is the time that the production test system is ready to test or is testing parts.

Contactor cleaning and rebuild, along with test cell changeover and test-cell setup, are necessary conditions that require test cell downtime.

Contactors that can be cleaned quickly and require less frequent cleaning increase test-cell availability.

When using gold-plated pins with tin alloy solders, a contactor with a self-cleaning feature can help reduce the frequency of contactor cleaning. A self-cleaning feature will also help delay amalgamation between the gold plating and tin.

Contactor rebuilding or replacement also causes test cell downtime. Contactors that have long mechanical life and can be quickly and easily rebuilt increase test cell availability.

Contactors that can be easily rebuilt reduce rebuild errors that could increase test-cell downtime. The life of the contact pin also contributes to the number of devices tested prior to contactor rebuild.

NiPdAu is much harder than tin-lead and may cause the contact-pin surface and plating to wear prematurely. Using lower forces and a harder contact-pin material can extend contact pin life on NiPdAu I/O platings.

Plating a softer contactor base material, such as BeCu with a harder material—palladium, for example—may not be a good solution, since the plating may fatigue, crack, flake away or wear away from the base material.

To extend the mean time between rebuilding, and therefore increase test cell availability, contact pins should be made of heavy precious metal element alloys.

Test Cell Performance Rate

Performance rate is the ratio of how long the test cell is actually running to its full potential for the individual device types being tested and sorted and represents the speed or throughput in number of units tested per hour.

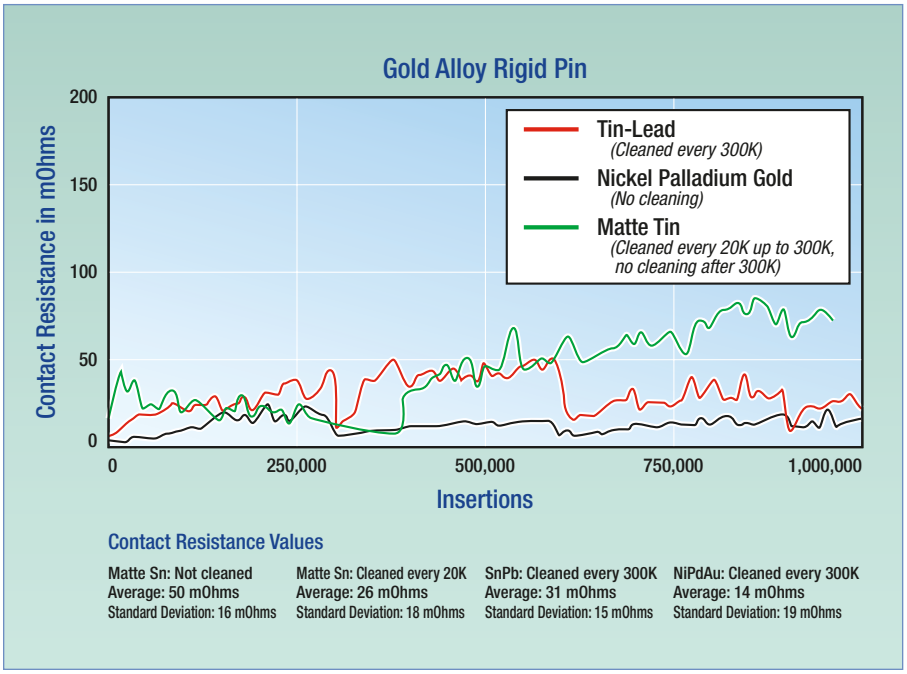


Figure 4. Contact resistance graphics for a variety of device I/O platings

This rate is the efficiency element and is, therefore, sometimes referred to as the *throughput efficiency* or *performance efficiency*.

The performance rate is the ideal optimized test-program time plus the ideal handler-index time multiplied by the total devices to be tested. Efficiency compromises come in all shapes and forms.

Wait states accommodate contactor-induced signal bounce or ground bounce relative to AC parametric testing of the device. Wait states are additive; they increase the test time per device tested and reduce the number of parts tested per hour. On the DC side, there may be a widening of measurement ranges to accommodate contactor resistance variances.

The performance limits of a contactor should not define the efficiency of the Pb-free test cell. Electrical, mechanical and thermal performance levels of contactors testing Pb-free devices should be equal to or better than tin-lead contacting technology.

Quality Rate

The quality rate, typically referred to as *yield percentage*, is the quantity of parts tested good, divided by the total number of parts tested.

The yield is the true throughput number; the parts that fail are a loss. Retested parts are also a loss of available capacity.

Test cell operators typically deal with declining yields by cleaning or rebuilding the contactor. Failures caused by associated items are called dependent failures.

Most false failures in Pb-free production test are dependent failures, since they are caused by the items associated with the I/O Pb-free plating or the contact pin geometry, alloy, plating, motion or bias force.

The performance limits of a contactor should not define the efficiency of the Pb-free test cell.

Conclusion

To satisfy the quality measures and throughput requirements for Pb-free production testing, the basic contacting principles described earlier in this article must be applied.

First, identify any accelerated performance deterioration (e.g., rapid solder build-up or rapid contact-pin wear) with the current system.

Maintain Precision

Next, keep the precision of the test cell at its proper level. Do not subordinate the performance of the test system to a low-performance, Pb-free contacting solution.

And keep the precision of the device-under-test interface at the proper level, including device lead backers, nests, ledges and plungers.

Finally, understand the packaged device's Pb-free plating and characteristics, and use these characteristics to select the right contactor with the right contact pins.

Mr. Brost is business development director for Johnstech. Previous management responsibilities include positions with Control Data Corporation, Sick Optik Elektronic, and Micro Component Technology. He holds a bachelor's degree in Business from Metropolitan University (St. Paul, Minn.), an MBA from the University of St. Thomas and several technology-based degrees. [bhbrost@johnstech.com]

Mr. Faller is Johnstech's product engineering manager. He has spent most of his career in Southern California working as a microwave/RF engineer in the aerospace and defense industries. He holds bachelor's and master's degrees in electrical engineering from the South Dakota School of Mines and Technology. [hlfaller@johnstech.com]